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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/901,280	07/09/2001	Giuseppe Rossi	08305-116001/20-31	7560

7590 10/20/2004

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EXAMINER	
TRAN, NHAN T	

ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 10/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/901,280	ROSSI ET AL.	
	Examiner	Art Unit	
	Nhan T. Tran	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2004 and 14 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23,25,26,28-32 and 34-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23,25,26,28-32 and 34-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/6/2004 and 6/14/2004 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 1-23, 25, 26, 28-32 and 34-36 have been considered but are moot in view of the new grounds of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-15, 25, 26, 28-32 & 34-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nair et al (US 6,366,320) in view of Takahashi et al (US 4,551,634).

Regarding claim 1, Nair discloses an apparatus comprising:

groups of image sensors (one group corresponds to each multiplexer 130 to 179 of a first level multiplexing), each group comprising subgroups (columns) of sensors (see Fig. 1; col. 1, lines 10-29; col. 3, lines 48-56, wherein the storage array 110 is also a sensor array);

subgroup select circuits (gate pairs in multiplexers 130 to 179), each of which is coupled to outputs from a respective subgroup of sensors (see Fig. 1; col. 3, lines 44-56);

group select circuits (gate pairs in multiplexers 180 to 186), each of which is coupled to outputs from subgroup select circuits associated with a respective one of the groups (Fig. 1);

a first bus for each group coupled to the outputs of the associated subgroup select circuits (i.e., a bus between 130 and 180; Fig. 1);

a controller (192) for providing control signals to the subgroup select circuits and the group select circuits to selectively enable the respective subgroup select circuits and group select circuits to pass signals from the sensors to a readout circuit (122, 126) one sensor at a time (sequential outputting/multiplexing of pixel by pixel, column by column) as shown in Fig. 1; col. 3, line 48 – col. 4, line 25;

a first isolation circuit (each gate pair in multiplexers 180 to 186) coupled to each first bus for selectively isolating each group from the readout circuit (e.g., turning on and then off each gate pair of multiplexers 180 to 186 in column by column basis). See Fig. 1; col. 3, line 48 – col. 4, line 25.

Nair fails to explicitly teach that the first isolation circuit comprising a switch for selectively connecting the first bus to a predetermined voltage. Takahashi teaches a multiplexing circuit in which a third transistor (23-x) is added in addition to a pair of transistors (21-x and 22-x) to clamp the voltage level of each non-selected channel (isolated bus) to ground so that mutual interference such as noise, crosstalk between neighboring selected and non-selected channels are prevented. See Takahashi, Fig. 2, col. 1, lines 45-55 and col. 3, line 15 – col. 4, line 15.

Therefore, it would have been obvious to one of ordinary skill in the art to improve signal integrity of the analog multiplexer 118 in Nair by implementing a switch (i.e., a transistor) in the first isolation circuit for selectively connecting the first bus to a predetermined voltage (i.e., 0V ground) to eliminate mutual interference between neighboring buses in view of the teaching of Takahashi.

Regarding claim 2, Nair also refers that the sensors are active pixel sensors (col. 1, lines 16-20).

Regarding claim 3, Nair further discloses a second bus coupled to the outputs of the group select circuits and the readout circuit (i.e., a bus between 180 and 187 that is coupled to the readout circuit 122, 126 via 187).

Regarding claim 4, Nair discloses that the number of group select circuits is approximately equal to the square root of the number of the subgroup select circuits (col. 4, lines 3-10, wherein 7 second level muxes $\cong$ square root of 50 first level muxes).

Regarding claims 5 & 6, although Nair and Takahashi do not specifically disclose that a ratio of the number of subgroup select circuits to group select circuit is in a range of 15:1 and 30:1 as required in claim 6 (this is also within the range of 10:1 and 40:1 required in claim 5), Nair suggests, in col. 1, lines 29-37, that modern imaging arrays can be very large and future arrays are expected to be even larger which requires modification on circuit design. Therefore, it would have been obvious to one of ordinary skill in the art to implement a ratio of the number of subgroup select circuits to group select circuit in a range of 10:1 and 15:1 as an obvious variation depending on the actual size of the sensor device.

Regarding claim 7, in col. 4, lines 3-10 and Fig. 1, Nair discloses that the 32 predetermined coded lines selects one of 16 pass gate pairs in the selected first level mux, a corresponding one of 8 pass gate pairs in the selected second level mux, and finally a corresponding one of 8 pass gate pairs in the third level mux. It is implied that when one gate pair in the multiplexer 180 corresponding to the 16 gate pairs in the multiplexer 130 is **ON**, the 16 gate pairs are also sequentially **ON** to pass the signals from the 16 gate pairs to the first bus between the 130 and 180 for the multiplexers sequentially output signals. When the signals output from the 16 gate pairs are done, the corresponding gate pair in the multiplexer 180 must be **OFF** and a next gate pair of the 8 gate pairs in the multiplexer 180 is **ON** to sequentially receives output signals from the next corresponding 16 gate pairs (i.e., 131) and so on. Thus, each group select circuit of 180 comprises at least a transistor switch with a respective gate terminal (either a full CMOS gate or a half gate) for receiving a control signal from the controller

(192), wherein when the switch is turned on, the group select circuit is enabled to pass signals from associated subgroup select circuits to the first bus, and when the switch is turned off, the group select circuit is disabled from passing signals from the associated group select circuits to the first bus.

Regarding claim 8, see the analysis in claim 7 for the similar structure and operations of each subgroup select circuit.

Regarding claim 9, Nair discloses that the controller (192) is configured for generating the control signals (by decoding 10 bit column address) to enable and disable the group select circuit switches and the subgroup select circuit switches in a predetermined sequence (col. 3; line 57 – col. 4, line 10 and note that a predetermined sequence is pixel by pixel in column by column basis as described in col. 3, lines 42-46).

Regarding claim 10, Nair also discloses that the controller is configured to provide the control signals to enable the switches in the group select circuits sequentially, and, while a particular group select switch is enabled, to enable the subgroup select circuits associated with the particular group select circuit sequentially, one at a time (Fig. 1; col. 4, lines 3-10 and the Examiner's analysis in claims 1, 7 & 9 are also applied here).

Regarding claim 11, see the analysis in claim 9.

Regarding claim 12, although Nair and Takahashi do not specifically disclose that each group select circuit comprises a pair of NMOS transistor switches, Nair suggests that each pair can be a full CMOS transmission gate (comprises a complementary pair of a NMOS and a PMOS transistor), a half gate (either a pair of PMOS transistors or a pair of NMOS transistors) or any other device that acts as a switch (col. 3, lines 52-56).

Therefore, it would have been obvious to one of ordinary skill in the art to implement the switches by using NMOS switches instead of a full CMOS switches in view of the suggestion of Nair in an obvious configuration for the transmission gates. *It should be noted that the third transistor taught in Takahashi is not considered as a transmission gate. It is simply a switch to ground.*

Regarding claim 13, Nair further discloses supergroups of sensors (all sensors that correspond to *each* of multiplexers 180 to 186; Fig. 1);

supergroup select circuits (gate pairs in multiplexer 187), each of which is coupled to outputs from group select circuits associated with respective one of the supergroups;

a second isolation circuit (also, gate pairs in multiplexer 187) coupled to each second bus (i.e., a bus between 180 and 187) for selectively isolating each supergroup from the readout circuit;

wherein the controller is configured to provide control signals to the supergroup select circuits to selectively enable a supergroup select circuit to pass a signal from the second bus to a third bus (i.e., a bus between 187 and 122) which is a common output bus (see Fig. 1 and the Examiner's analysis in claims 1, 3, 7 & 9).

Although Nair does not teach the second isolation circuit comprising a switch for selectively connecting the first bus to a predetermined voltage, a similar motivation and modification as expressed in claim 1 is further applied to the second isolation circuit in view of the teaching of Takahashi to maintain signal integrity throughout the multiplexer 118.

Regarding claim 14, it is shown by Nair, Fig. 1 at multiplexer 187 that an output of each supergroup select circuit is electrically coupled to a common output bus.

Regarding claim 15, see claim 7 for the similar analysis for a transistor switch with a respective gate terminal for receiving a control signal from the controller.

Regarding claim 25, see the analysis of apparatus claim 1.

Regarding claim 26, Nair discloses the step of amplifying the readout signals from the array (col. 4, lines 22-25).

Regarding claim 28, see the analysis in claim 13.

Regarding claim 29, Nair clearly discloses a step of coupling each supergroup select circuit (gate pairs in multiplexer 187) to an associated second bus (i.e., a bus between 180 and 187), wherein the readout signals from each sensor in the supergroup inherently travel through the second bus as shown Fig. 1 and col. 3, lines 48-56.

Regarding claim 30, see the analysis of claim 13.

Regarding claim 31, see the analysis in claim 1 and Fig. 1, wherein each group comprises a plurality of columns of an image sensor array, and a plurality of column select circuits, each of which coupled to an output from a column of sensors (col. 3, lines 48-56).

Regarding claim 32, see the analysis in claim 2.

Regarding claim 34, see the analysis in claims 1 & 13. Note Fig. 1 for at least two group buses (i.e., buses between 130-179 and 180-186), each group bus coupled to outputs of the subgroup select circuits (130-179) associated with respective group.

Regarding claims 35 and 36, as clearly taught by Takahashi, the predetermined voltage is a ground potential. See Takahashi, col. 3, lines 49-52 and col. 4, lines 10-15.

4. Claims 16 – 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nair et al (US 6,366,320) in view of Barcella (US 5,715,204).

Regarding claim 16, see the analysis of apparatus claim 1 with respect to Nair's disclosure for sequentially multiplexing the output signals of the sensor array. However, Nair fails to suggest that the sense amplifier (116) is placed after the multiplexer (118) to enable a un-

amplifier pixel output signal to be multiplexed by the multiplexer (118). Barcella teaches an alternative arrangement of a sense amplifier (630) that is placed after a column multiplexer (620). See Barcella, Fig. 6.

Therefore, it would have been obvious to one of ordinary skill in the art to alternatively configure the circuit arrangement in Nair by amplifying an un-amplified pixel signal after multiplexing instead of before multiplexing to reduce a number of sense amplifiers.

Regarding claim 17, see the analysis of claim 16 and note that Nair teaches a controller (192) for providing control signals to sequentially select subgroup and group (sequential outputting/multiplexing of pixel by pixel, column by column) as analyzed in claim 1 and shown in Fig. 1; col. 3, line 48 – col. 4, line 25.

Regarding claim 18, see the analysis of claim 16, wherein each gate pair in multiplexers 180-186 corresponding to each first level multiplexing at 130-179 is sequentially disabled to produce a pixel signal chain as shown in Nair.

Regarding claim 19, see the analysis of claim 16. Furthermore, a supergroup select circuit is represented by each gate pair in the multiplexer 187 as shown by Nair in Fig. 1

Regarding claims 20 - 23, see the analysis in claims 17 & 18 for the similar operations at the third level of multiplexing at 187 and in combination with the second and first level of multiplexing (Nair, col. 4, lines 3-10).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (703) 605-4246. The examiner can normally be reached on Monday - Thursday, 8:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew B Christensen can be reached on (703) 308-9644. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NT.

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